REMARKS

Claims 1-14 are pending in this application. By this Amendment, the Abstract of the Specification and claims 1-3, 5, 7 and 9 are amended. Claims 11-14 are added.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

With respect to the prior art rejections, claims 1-3 and 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamamoto (U.S. Patent No. 6,064,079). Claims 4-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto as applied to claim 1 above and further in view of Fukuda (U.S. Patent No. 6,872,986). Claims 7-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Kaneyama (U.S. Patent Application Publication No. US 2002/0014632).

The rejection is respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The invention of claim 1, for example, is directed to a group III-nitride-based compound semiconductor device, that includes a first p-layer and a second p-layer, the first p-layer and the second p-layer including an acceptor impurity, and an intermediate layer provided between the first p-layer and the second p-layer. The intermediate layer includes a donor impurity at a concentration distribution that is based on activation rates of the acceptor and the donor impurities. (Application at page 3, lines 4-15).

This structure is important because by compensating for the concentration of the acceptor impurity, a hole concentration in the intermediate layer is substantially the same as that in a group III-nitride-based compound with no impurity added (Application at page 3, lines 16-25).

In a conventional group III-nitride-based semiconductor, as described in the Background of the present Application, the ability to withstand electrostatic voltages is far less than that of gallium-arsenic-based or an indium-phosphorous-based LED. Moreover, attempts to increase the ability to withstand electrostatic voltages has only resulted in a

concomitant increase in resistivity and thickness (Application at page 1, line 14-page 2, line 18).

In contrast, an exemplary aspect of this invention may improve the ability to withstand electrostatic voltages, as well as reduce a driving voltage (Application at page 2, line 21-page 3, line 3).

II. THE PRIOR ART REJECTION

A. The 35 U.S.C. §102(b) Yamamoto reference rejection

In rejecting claims 1, 2, 3 and 6 under 35 U.S.C. §102(b), the Examiner alleges that Yamamoto et al. (Yamamoto) discloses or suggests each and every feature recited in the rejected claims. However, there are features of the rejected claims that are neither disclosed nor suggested by Yamamoto.

For example, Yamamoto fails to disclose or suggest an intermediate layer provided between the first p-layer and the second p-layer or that the intermediate layer includes a donor impurity at a concentration distribution that is based on activation rates of the acceptor and the donor impurities.

Yamamoto discloses a gallium nitride-based compound semiconductor device that has a p-type cladding layer 15 and a p-type low resistivity layer 16. Both of the layers 15 and 16 are doped with Mg (col. 4, lines 28-45 of Yamamoto). A current blocking layer 17, having a striped open portion that forms a current path is also included in the device of Yamamoto.

In an embodiment, Yamamoto further describes a p-type modulation layer 34, that is doped with Si, formed "inside the p-type low resistivity layer 16 in a manner to the open portion" (col. 5, lines 27-60).

The Examiner alleges that the current blocking layer 17 and the p-type modulation layer 34 correspond to the claimed intermediate layer. However, Yamamoto is silent regarding an intermediate layer (the current blocking layer 17 and the p-type modulation layer 34 of Yamamoto) that takes into account the activation rate of the dopants.

Instead, Yamamoto merely recites that the p-type modulation layer 34 contains a concentration of Si in addition to a predetermined concentration of Mg. The distribution of Si is concentrated in a single region at a central portion of the p-type modulation layer 34, as shown in Fig. 2B of Yamamoto. The concentration of Si at the central portion acts as a high resistivity region having a low p-type carrier concentration (col. 5, lines 37-56).

Thus, Yamamoto fails to disclose or suggest an intermediate layer provided between the first p-layer and the second p-layer or that the intermediate layer includes a donor impurity at a concentration distribution that is based on activation rates of the acceptor and the donor impurities.

As Yamamoto fails to disclose or suggest all of the features of the rejected claims, withdrawal of the rejection is respectfully requested.

B. **The 35 U.S.C. §103(a) Yamamoto and Fukuda reference rejection**

In rejecting claims 4 and 5 under 35 U.S.C. §103(a), the Examiner alleges that the combination of Yamamoto and Fukuda discloses or suggests each and every feature recited in the rejected claims. Applicants submit that claims 4 and 5 are allowable for their dependency on independent claim 1 for the reasons discussed above, as well as for the additional features recited therein.

The Examiner admits that Yamamoto fails to disclose the additional features recited in dependent claims 4 and 5. In an effort to overcome the admitted deficiency, the Examiner combines Fukuda for allegedly teaching such features.

However, Fukuda is not available as prior art and therefore, a *prima facie* case of obviousness has not been established.

Fukuda fails to qualify as prior art under 35 U.S.C. §102 because Fukada was not published in English under PCT Article 21(2) prior to the September 16, 2003 filing of JP 2003-322541, from which the present Application claims priority. Specifically, Fukada was first published in the English language on August 12, 2004, which date is subsequent to the September 16, 2003 priority date of the present Application. In this case, the original publication date of Fukada on January 16, 2003 was in Japanese and not in English.

As Yamamoto fails to disclose or suggest the features of claims 4 and 5, withdrawal of the rejection is respectfully requested.

C. **The 35 U.S.C. §103(a) Yamamoto and Kaneyama reference rejection**

In rejecting claims 7-10 under 35 U.S.C. §103(a), the Examiner alleges that Yamamoto discloses all of the recited claim features except "that the p electrode comprises a thin film electrode and a thick film electrode." In an effort to overcome the admitted deficiencies, the Examiner combines Kaneyama.

However, as discussed above, Yamamoto fails to disclose or suggest an intermediate layer provided between the first p-layer and the second p-layer or that the intermediate layer includes a donor impurity at a concentration distribution that is based on activation rates of the acceptor and the donor impurities.

Kaneyama discloses a group III nitride semiconductor device that includes p-type contact layer 109 disposed on a p-type clad layer 108. Kaneyama fails to disclose or suggest an intermediate layer between the p-layers 108, 109, or concentrations of donor and acceptor impurities in such an intermediate layer.

As such, Kaneyama fails to overcome the deficiencies of Yamamoto and the combination of references fails to disclose or suggest each and every feature recited in the rejected claims.

Therefore, withdrawal of the rejection of claims 7-10 is respectfully requested.

III. Formal Matters

A. New Claims

New claims 11-14 are not anticipated or rendered obvious by the applied references, whether considered alone or in combination.

B. **Conclusion**

In view of the foregoing, Applicants submits that claims 1-14, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 12/9/06

John W. Fitzpatrick, Esq.
Registration No. 41,018

Sean M. McGinn, Esq.
Registration No. 34,386

MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182-3817
(703) 761-4100
Customer No. 21254

Substitute Abstract

In a group III-nitride-based compound semiconductor device, an intermediate layer is provided between a p-AlGaN layer and a p-GaN layer, to each of which an acceptor impurity is added. On this occasion, the intermediate layer is doped with a donor impurity in a concentration, by which holes generated by an acceptor impurity introduced into the intermediate layer during the formation of the p-AlGaN layer are substantially compensated. As a result, the conductivity of the intermediate layer becomes extremely low, and therefore the electrostatic withstand voltage of the group III-nitride-based compound semiconductor device improves significantly.